proportional to the ratio of the majority carrier doping concentrations at each side of the space charge region. Thus, the reverse conduction condition is different along the bulk of the device. The level of minimum contact potential at the blocking junction is obtained at some distance from the surface. This is the place where the initial reverse conduction by impact ionization and tunneling gives rise to the next path for current conduction deep in the bulk of the device. This tunable effect provides a strength of the proposed ESD protection cell. Once the potential barriers reach the conduction conditions, the STT is able to open multiple high conduction paths.

[0086] The holding voltage after triggering is an integral function of the electric field distribution between the two terminals of the device, including primarily the voltage in the space charge neutral region where carriers are injected from both sides of the device. If the distance between the anode and cathode is increased, the holding voltage is increased as well but some characteristics in the device may be degraded. Likewise, higher injection of carriers increases the injection efficiency, and the device can be turned-on earlier but the voltage also snaps back to a lower holding voltage. One way to obtain the optimum design is to find the compromise solution that controls the trigger and the voltage in the junctions by using the appropriate lateral dimensions of the device and the appropriate dimensions for the anode and cathode contacts in order to avoid a very high injection in the anode but without violation of the design rules. The low on-state voltage in the blocking junction, the creation of a region of quasi-neutral electron-hole plasma along the junction, and a better distribution of the electric field along the device and deeper in the bulk are some of the further advantages of the STTs that allow a better performance at high current conditions and in a lower power dissipation per unit area than existing ESD protection methods.

[0087] For the STTs with n-side of the guard-ring (N-Tub) floating (see **420** in FIGS. **4**B and **4**C), the transverse area for current flux between anode and cathode is narrower. For the SSTT, the forward conduction is depicted in FIGS. **11**A and **11**B. These figures show the lateral and vertical PNP BJTs with floating N-Well, (**16** in FIG. **6**A). The N-Well to P-Well (i.e. base-collector of the lateral BJTs in the anode) breakdown is due to instability caused by carrier avalanche multiplication at the distributed PNP BJT. Similar to the case previously described, electrons are generated by impact ionization of holes injected in the collector-base (CB) junction and it contributes to an effective base current, which in turn controls hole injection across the emitter-base (EB) diode. This situation creates a feedback system where the collector current is related to the effective base current, which is composed of one terminal current, the thermal generation of holes within the shunt lateral transistors, and the feedback component due to the impact ionization of injected electrons as well as by the forward gain which is characterized by the emitter efficiency.

[0088] In this device, the conditions for the trigger voltage are similar to those previously detailed for the device with the N-Tub tied to the anode. However, the effective resistance is smaller and also the voltage that can be withheld along the device is smaller. This effect along with the open base conditions in the PNP in the anode side give rise to smaller holding voltages and slightly smaller trigger voltages.

[0089] In general, for both interconnection conditions previously presented, in addition to the sustained high injection condition after snapback, a so called dual-carrier-injection is also present in the total current density. In this condition, a drift current density due to the majority carriers of both kinds—holes and electrons—gives rise to a quasi-neutral electron-hole plasma that controls the electric field in the junction. A second component given by carrier diffusion is important during the triggering process but less important during the 'on' condition of the device, and a final component due to tunneling effects may be present at the blocking junction during the on-state high-current regime. Additionally, the relationship between resistance and current is not a mutually exclusive multiplication of two constants, but the current density modulates the conductance. Therefore, the on-state I-V characteristics are also affected by the modulation of the conductivity, which changes with the device interconnections and with the lateral dimensions.

[0090] The STT's I-V characteristics are designed for different I/O pad and supply clamp conditions by adjusting the internal lateral dimensions. The holding voltage can be dependent on: 1) the dimension 'D**1**' (**22** in FIGS. **5**A and **6**A and **24** in FIGS. **5**B and **6**B); 2) the size and equivalent resistance of the anode contact (**32** in FIGS. **5**A and **6**A and **28** in FIGS. **5**B and **6**B); 3) the dimension L in the DSTTs (**42** in FIGS. **5**A and **44** in FIG. **5**B) and in the SSTTs (**40** in FIGS. **5**A and in **5**B); and 4) the equivalent resistance of the intermediate N-Well in the anode side.

[0091] The holding voltage increases with an increase in D**1**, reduction of emitter contact size, which provides emitter injection control, an increase in the channel length, and a reduction in the equivalent N-Well resistance. Increasing the length D**1** affects the way that the N-Well to P-Well blocking junction is conducting during the on-state.

[0092] As the distance D**1** increases, the well-known model of the SCRs formed by two BJTs is no longer valid. Therefore, voltages higher than that obtained by just two forward-biased junctions can be tuned along the device. This tunable holding voltage is sustained in the blocking junction and to some extent by the distributed BJT and passive network in the bulk of the device.

[0093] When the holding voltage is increased, the effective conduction path is shrunk to a more superficial region, the maximum current that the cell can support is lower, but the maximum effective power before a hard failure occurs in the device is almost independent of changes in the lateral dimensions. The reduction of the hard-failure maximum current when the holding voltage is increased is an unavoidable trade-off, but even at relatively high holding voltages, the design with STTs provides a much more efficient and robust protection scheme for standard digital circuits. The STTs are also the first reliable devices designed for the protection of ICs with I/O voltages much higher than the core circuit power supply and at levels where devices with gate cannot be used.

[0094] The tendency previously discussed is observed in various STTs. For devices with floating N-Tub though, a lesser adjustment at high holding voltages level is possible due to the open-base BJTs existent in the anode of the STTs.

[0095] The reverse characteristics of the STTs are not dependent on the internal lateral dimensions, but on the